EXPRESS MAIL NO. EV064844937US

FORM PTO-1390 (REV 11-2000) DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.
851663.434USPC

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
Unknown 10/089535

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SG99/00095	29 September 1999 (29.09.99)	NA

TITLE OF INVENTION
MULTIPLE INSTANCE IMPLEMENTATION OF SPEECH CODECS

APPLICANT(S) FOR DO/EO/US
TIAN, Wenshun; LEONG, Foo Yuen and ALVAREZ-TINOCO, Antonio Mario

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4)
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items of information:

U.S. APPLICATION NO. (Known if assigned) (37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unknown 10/089535	PCT/SG99/00095	851663.434USPC

21. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)..... $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$130.00	

Claims	Number Filed	Number Extra	Rate		
Total Claims	16 - 20 =	0	x $ 18.00	$0.00	
Independent Claims	4 - 3 =	1	x $ 84.00	$84.00	
Multiple dependent claim(s) (if applicable)			+ $280.00	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$1,104.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$0.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$0.00	
TOTAL NATIONAL FEE =				$1,104.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$0.00	
TOTAL FEES ENCLOSED =				**$1,104.00**	
				Amount to be refunded:	
				charged	

a. ☒ A check in the amount of $1,104.00 cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. in the amount of $_ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **19-1090**. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

Robert Iannucci
NAME

33,514
REGISTRATION NUMBER

EXPRESS MAIL NO. EV064844937US

PATENT COOPERATION TREATY

Int'l Application No.	:	PCT/SG99/00095
Int'l Filing Date	:	29 Septembger 1999
U.S. Application No.	:	Not yet known
Inventors	:	TIAN, Wenshun et al.
Title	:	MULTIPLE INSTANCE IMPLEMENTATION OF SPEECH CODECS
Docket No.	:	851663.434USPC
Date	:	28 March 2002

Box PCT
Assistant Commissioner for Patents
Washington, DC 20231-0001

PRELIMINARY AMENDMENT

Sir:

Applicants respectfully request entry of preliminary amendments in the above-identified United States National Phase patent application. Please amend the claims as follows:

In the Claims:

Please amend Claims 3, 5, 6, 10, 12 and 13 as follows:

3. (Amended) A method as claimed in claim 1, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

5. (Amended) A method as claimed in claim 1, wherein each of the memory segments in said second memory is the same size.

6. (Amended) A method as claimed in claim 1, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

10. (Amended) A system as claimed in claim 8, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec

instance to modify addressing of variables for that codec instance to the corresponding memory segment.

12. (Amended) A system as claimed in claim 8, wherein each of the memory segments in said second memory is the same size.

13. (Amended) A system as claimed in claim 8, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

REMARKS

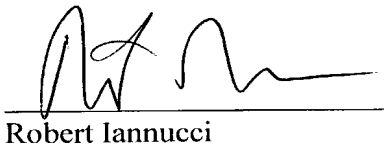
Claims 1-16 will be pending upon entry of the present amendment. Claims 3, 5, 6, 10, 12 and 13 are being amended.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**."

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC



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Enclosure: Appendix

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 3, 5, 6, 10, 12 and 13 as follows:

3. (Amended) A method as claimed in claim 1 ~~or 2~~, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

5. (Amended) A method as claimed in ~~any one of~~ claims 1 ~~to 4~~, wherein each of the memory segments in said second memory is the same size.

6. (Amended) A method as claimed in claim 1~~, 2, 3, or 4~~, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

10. (Amended) A system as claimed in claim 8 ~~or 9~~, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

12. (Amended) A system as claimed in ~~any one of~~ claims 8 ~~to 11~~, wherein each of the memory segments in said second memory is the same size.

13. (Amended) A system as claimed in ~~any one of~~ claims 8 ~~to 11~~, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

MULTIPLE INSTANCE IMPLEMENTATION OF SPEECH CODECS

Field of the Invention

This invention relates to audio coding, and is particularly applicable in the field of telecommunication and the internet, for example, in which multi-channel speech coders are implemented using a single digital signal processing (DSP) device.

Background

Because of the computationally expensive nature of encoding and decoding real-time audio, traditionally audio coders/decoders ("codecs") have been implemented by specialized integrated circuit chips. An alternative is to provide the audio codec functions in software (firmware, micro-code, etc.) for operation on a more general purpose Digital Signal Processor ("DSP"). With the deployment of more powerful Digital Signal Processors, it can be possible for more than one codec to be real-time implemented using a single DSP chip. For example, it may be possible for a powerful DSP to process a plurality of different audio signals or channels in real-time, to thereby implement a plurality of voice coders ("vocoders") using a single processing device.

Summary of the Invention

In accordance with the present invention, there is provided a method for implementing a plurality of encoders and/or decoders (codecs) using a single digital signal processing (DSP) device, wherein the function of each codec is performed by the DSP according to an instruction code program, the method comprising the steps of:

providing an instruction code program stored in a first memory for controlling the DSP to function as a codec;

providing a second memory including a plurality of memory segments;

implementing a plurality of codecs using the DSP by running said instruction code program in the first memory a plurality of times in re-entrant instances, wherein each codec instance is provided access to a respective separate memory segment in the second memory for storing data used in encoding/decoding a respective separate data stream.

The present invention also provides a data coding and/or decoding system in which a plurality of encoders and/or decoders (codecs) are implemented using a single digital signal processing (DSP) device, comprising:

a digital signal processor (DSP);

a first memory coupled to the DSP and containing an instruction code program, the function of each codec being performed by the DSP, in use, according to the instruction code program;

a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments;

wherein a plurality of codecs are implemented using the DSP by running the instruction code program in the first memory a plurality of times in re-entrant instances, and wherein each codec instance is provided access to a respective separate memory segment in the second memory for storing data used in encoding/decoding a respective separate data stream.

Preferably a third memory is also provided which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

Each codec instance preferably accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

In a preferred form of the invention the plurality of memory segments are contiguous in the second memory, and the at least one index register is set for each codec instance according to

an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codec instance. Preferably each of the memory segments in said second memory is the same size.

In one form of the invention, the first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, wherein different codec instances may be selected from the different kinds of codec. Preferably, then, each of the memory segments in the second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codec.

This methodology can be used to modify the existing DSP assembly code or to implement a new algorithm with a multiple instance feature. The multiple-instance implementation can be used to process multi-channel signals using one software module.

Brief Description of the Drawings

The invention is described in greater detail hereinafter, by way of example only, with reference to preferred embodiments thereof and the accompanying drawings, in which:

Figure 1 is a block diagram of a simple audio encoding system employing a DSP;

Figure 2 is a block diagram of a data memory structure for a first embodiment of the present invention; and

Figure 3 is a block diagram of a data memory structure for a second embodiment of the invention employing a plurality of different codec types.

Detailed Description of the Preferred Embodiments

The embodiments of the invention described hereinbelow are in the context of audio coders implemented by instruction codes in the form of software, firmware or micro-code operating

on a general purpose digital signal processor chip. In particular, the described embodiments relate to implementation of speech codecs of the type which is the subject of ITU-T Recommendation G.729. However, it will be appreciated by those of ordinary skill in the art that the present invention is not necessarily limited to such an environment, and may further be used to implement coders for other forms of real-time data streams including other forms of voice and/or facsimile transmission or storage coding.

A simple audio encoding system 10 based on a general purpose DSP is illustrated in block diagram form in Figure 1. The audio coding system 10 comprises a digital signal processor (DSP) 12 which is coupled to receive input data and produce coded output signals. The DSP 10 is coupled to a storage memory 14. The memory 14 provides data to the DSP 12 to enable coding of the received input data to take place. The memory 14 may contain various different forms of data, including read-only data which is permanently stored in the memory, and temporary data which is transiently stored during coding operations. The memory 14 may also contain stored instruction codes used by the DSP to perform the coding, which would ordinarily be permanently stored in read-only form.

One of the considerations which must be dealt with in implementing multiple codecs on a single DSP by operating multiple instances of the DSP instruction codes which control the codec operation is the arrangement of storage memory so that each instance of the codec can have efficient memory usage and not interfere with other codec instances in use at the same time. In accordance with an embodiment of the present invention, this is achieved by arranging the data memory as illustrated in the block diagram of Figure 2. This exemplary embodiment relates to implementation of a 4-channel multiple instance vocoder on a single DSP. As shown in Figure 2, the data memory is partitioned into different parts, in this case comprising read-only memory (ROM), local RAM, and static RAM. The ROM is used to store all the read only data, which may include the program instruction codes and the like. Local RAM is used for storage of temporary variables and for data buffering. The static RAM, on the other hand, is used for storage of all the global and historical variables required for the coding operations, for example

data which will be used for processing the next frame of output. As shown in the block diagram, in this case the static RAM is partitioned into separate areas for each DSP codec instance. Thus, static RAM_i is constrained for use only by the i^{th} coder (i = 1, 2, 3, 4), while the data ROM and local RAM are shared by all four channels.

The preferred form of the present invention involves partitioning the data memory based on their properties and using an index register or index modifier to modify the address of the static RAM segment data used for each codec instance. The program code memory can be arranged as usual. If, however, program memory is used for data accessing, this part of memory also needs to be partitioned in the same way as data memory such as X or Y. This methodology allows the easy management of the operating system or real-time kernel due to the facility of opening and closing the various instances.

First, the partition of the data memory according to its accessing property is obtained, for example in the embodiment shown in Figure 2 involving ROM data, temporary local RAM, and static or global RAM segments. The data ROM and temporary local RAM are shared for every instance. Only the static RAM segments are used exclusively by corresponding codec instances. This static RAM segment is accessed using an *index register* by adding an offset value to address the static RAM segment for a particular instance. This is the basis of method to implement a new algorithm for multiple codec instances on a single DSP. Using this method, as described in greater detail below, existing DSP program instructions can be modified relatively easily to operate multiple codec instances.

When modifying existing DSP codes for multiple instance operation, it is not necessary to change all of the existing variable names using the arrangement of the data memory with partitions as described above. For static data memory access, it is only necessary to modify the existing addressing mode to obtain an indirect addressing scheme using the *index* and *address registers*. One example is shown in the Table below using a D950 DSP made by STMicroelectronics. For other DSPs, a similar approach can be employed. In the Table, ax0

is one of the address registers and ix1 and ix2 are index registers.

Before (non-re-entrance)		**Modified (re-entrance)**	
Direct var1.x = Register1	(note #1)	*Indirect* ax0 = #var1 *(ax0 + ix2) = Register1	(note #2) (note #3)
Indirect ax0 = #var10 Rep N times loop1 Register = *ax0+ix1 ... loop1	(note #2) (note #5) (note #6) (note #7)	*Indirect* ax0 = #var10 ax0 = ax0+ix2 Rep {N-1} times loop1 Register = *ax0+ix1 ... loop1	(note #2) (note #4) (note #5) (note #6) (note #7)

In order to pass the addressing information to every channel vocoder, two index registers should be reserved for this reentrant purpose, say IX2 and IY2 if using a D950 DSP. By doing so, the address of all the static variables stored in the respective static RAM segments will be modified by these two index registers from the beginning.

There are two methods by which stored data can be access from the static RAMs. One is direct addressing and the other is indirect addressing. However, for reentrant implementations, access to the static RAM must be through indirect addressing. Therefore, to achieve the reentrant feature and run multiple instance codecs, the existing instruction codes for the DSP should be modified accordingly, using the index register, indicated as an example in the Table above.

If the addressing instruction codes are modified accordingly and data memory is arranged as shown in the Figure 2, the multiple-instance 4-channel system can operate as follows,

Repeat following codes
/*first instance*/
Ix2=#offsetx$_1$
Iy2=#offsety$_1$
Call coder
/* second instance*/
Ix2=#offsetx$_2$
Iy2=#offsety$_2$
Call coder

/*third instance*/
Ix2=#offsetx$_3$
Iy2=#offsety$_3$
Call coder

/*fourth instance*/
Ix2=#offsetx$_4$
Iy2=#offsety$_4$
Call coder

where offsetx$_1$=offsety$_1$=0, offseti=addressx$_i$-addressx$_1$, offsety$_i$=addressy$_i$-addressy$_1$, for i=1, 2, 3. Address x$_i$ does not necessarily equal address y$_i$. One example of the static RAM size is about 1560 words in X memory and 256 words in Y memory for a codec operating according to ITU-T G.729. The static RAM size would typically be the same for each instance of the G.729 vocoder.

This is applicable for a new implementation or for converting existing DSP instruction coding to a re-entrant multiple instance implementation. Since this method does not require a change of the variable names in the DSP coding, it is efficient in both MIPS and porting

effort if compared to using pointers.

If there are more than one kind of speech codec in a system, the method described herein is still applicable. For a system using a plurality of different codecs, the memory may be arranged as illustrated in Figure 3, for which the multiple-instance accessing procedures are described below.

In Figure 3 the memory map for a 4-channel system is shown, in which the 4 active channels could be any possible combination of codecs operating according to ITU-T G729, G723.1 and FAX. In this case, the size of ROM segment comprises ROM data for all of the codec types. The size of the temporary local RAM segment is the maximum local RAM size used by any of the codecs. All of the different codecs share the local RAM segment. Similarly, each of the static RAM segments are of a size to accommodate the frame processing storage requirements of any one of the possible codecs implementations. This enables different codecs to make use of different static RAM segments.

One example is a 4-channel system with two different speech codecs, say G723.1 and G729. The program instruction codes are, in this example, stored separately in a program memory (not shown). The data memory is arranged as shown in Figure 3. Such a 4-channel system multiple instance system can operate as follows,

Repeat following codes
/*first instance*/
Ix2= #offsetx$_1$
Iy2= #offsety$_1$
If (codec_flag$_1$==CODEC1)
Call coder1
Else
Call coder2

/*second instance*/

Ix2=#offsetx$_2$

Iy2=#offsety$_2$

If (codec_flag$_2$==CODEC1)

Call coder1

Else

Call coder2

/*third instance*/

Ix2=#offsetx$_3$

Iy2=#offsety$_3$

If (codec_flag$_3$==CODEC1)

Call coder1

Else

Call coder2

/*fourth instance*/

Ix2=#offsetx$_4$

Iy2=#offsety$_4$

If (codec_flag$_4$==CODEC1)

Call coder1

Else

Call coder2

where offsetx$_1$=offsety$_1$=0, offsetx$_i$=addressx$_i$-addressx$_1$, offsety$_i$=addresy$_i$-addresy$_1$ for i=1, 2, 3. The flag variable *codec_flag$_i$* is writeable by an operating system or system controller, so as to dictate which type of codec is used for each instance.

The foregoing detailed description of the present invention has been presented by way of

example only, and many variations to the specific details therein may be apparent to those of ordinary skill in the art without departing from the scope of the invention. Accordingly, such specifics are not intended to be considered limiting to the scope of the invention which is defined in the appended claims.

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Claims

1. A method for implementing a plurality of encoders and/or decoders (codecs) using a single digital signal processing (DSP) device, wherein the function of each codec is performed by the DSP according to an instruction code program, the method comprising the steps of:

providing an instruction code program stored in a first memory for controlling the DSP to function as a codec;

providing a second memory including a plurality of memory segments;

implementing a plurality of codecs using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, wherein each codec instance is provided access to a respective separate memory segment in said second memory for storing data used in encoding/decoding a respective separate data stream.

2. A method as claimed in claim 1, wherein a third memory is provided which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

3. A method as claimed in claim 1 or 2, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

4. A method as claimed in claim 3, wherein the plurality of memory segments are contiguous in said second memory, and said at least one index register is set for each codec instance according to an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codec instance.

5. A method as claimed in any one of claims 1 to 4, wherein each of the memory segments in said second memory is the same size.

6. A method as claimed in claim 1, 2 3, or 4, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

7. A method as claimed in claim 6, wherein each of the memory segments in said second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codec.

8. A data coding and/or decoding system in which a plurality of encoders and/or decoders (codecs) are implemented using a single digital signal processing (DSP) device, comprising:

a digital signal processor (DSP);

a first memory coupled to the DSP and containing an instruction code program, the function of each codec being performed by the DSP, in use, according to said instruction code program;

a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments;

wherein a plurality of codecs are implemented using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, and wherein each codec instance is provided access to a respective separate memory segment in said second memory for storing data used in encoding/decoding a respective separate data stream.

9. A system as claimed in claim 8, including a third memory coupled to said DSP which is accessible by each of the codec instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams.

10. A system as claimed in claim 8 or 9, wherein each codec instance accesses the corresponding memory segment using indirect addressing based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codec instance to the corresponding memory segment.

11. A system as claimed in claim 10, wherein the plurality of memory segments are contiguous in said second memory, and said at least one index register is set for each codec instance according to an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codec instance.

12. A system as claimed in any one of claims 8 to 11, wherein each of the memory segments in said second memory is the same size.

13. A system as claimed in any one of claims 8 to 11, wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codec instances may be selected from the different kinds of codec.

14. A system as claimed in claim 13, wherein each of the memory segments in said second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codec.

15. A method for implementing a plurality of encoders and/or decoders (codecs) using a single digital signal processing (DSP) device, wherein the function of each codec is performed by the DSP according to an instruction code program, the method comprising the steps of:

providing an instruction code program stored in a first memory for controlling the DSP to function as a codec;

providing a second memory including a plurality of memory segments;

implementing a plurality of codecs using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, wherein each codec instance is provided access to a respective separate memory segment using an indirect addressing mode based on at least one index register in said second memory for storing data used in encoding/decoding a respective separate data stream.

16. A data coding and/or decoding system in which a plurality of encoders and/or decoders (codecs) are implemented using a single digital signal processing (DSP) device, comprising:

a digital signal processor (DSP);

a first memory coupled to the DSP and containing an instruction code program, the function of each codec being performed by the DSP, in use, according to said instruction code program;

a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments;

wherein a plurality of codecs are implemented using the DSP by running said instruction code program in said first memory a plurality of times in re-entrant instances, and wherein each codec instance is provided access to a respective separate memory segment using an indirect addressing mode based on at least one index register in said second memory for storing data used in encoding/decoding a respective separate data stream.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
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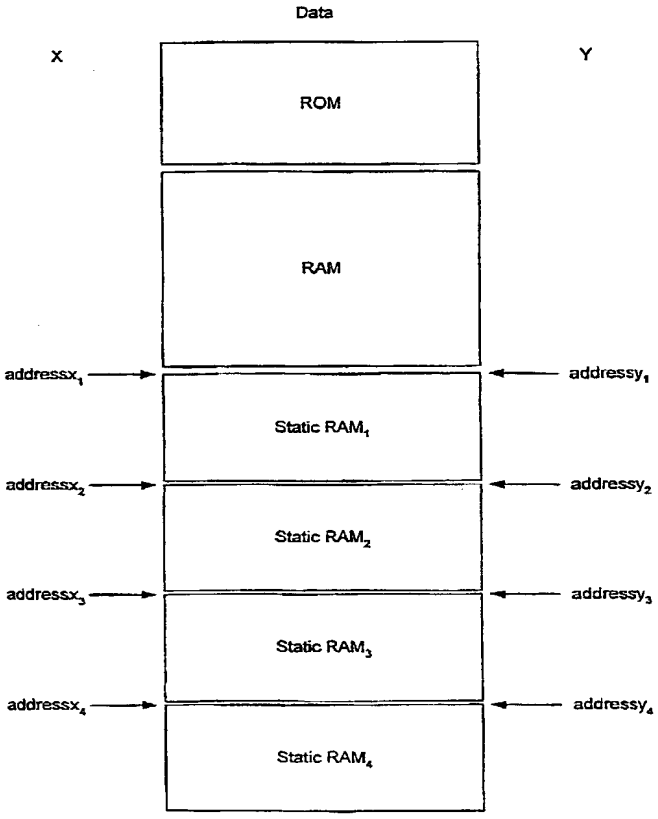
(54) Title: MULTIPLE INSTANCE IMPLEMENTATION OF SPEECH CODECS



(57) Abstract: A method for multiple instance implementation of speech codecs is described. By partitioning the data memory into ROM, local temporary RAM, and static RAM segments, a memory efficient multiple instance codec can be implemented. All the static memory segments are accessed by indirect addressing mode using index registers. A plurality of different codecs can also be implemented using the multiple-instance scheme. The described method provides a relatively easy way in which to implement multiple instance codecs or modify existing non-multiple instance implementations with the multiple instance feature for increased performance.

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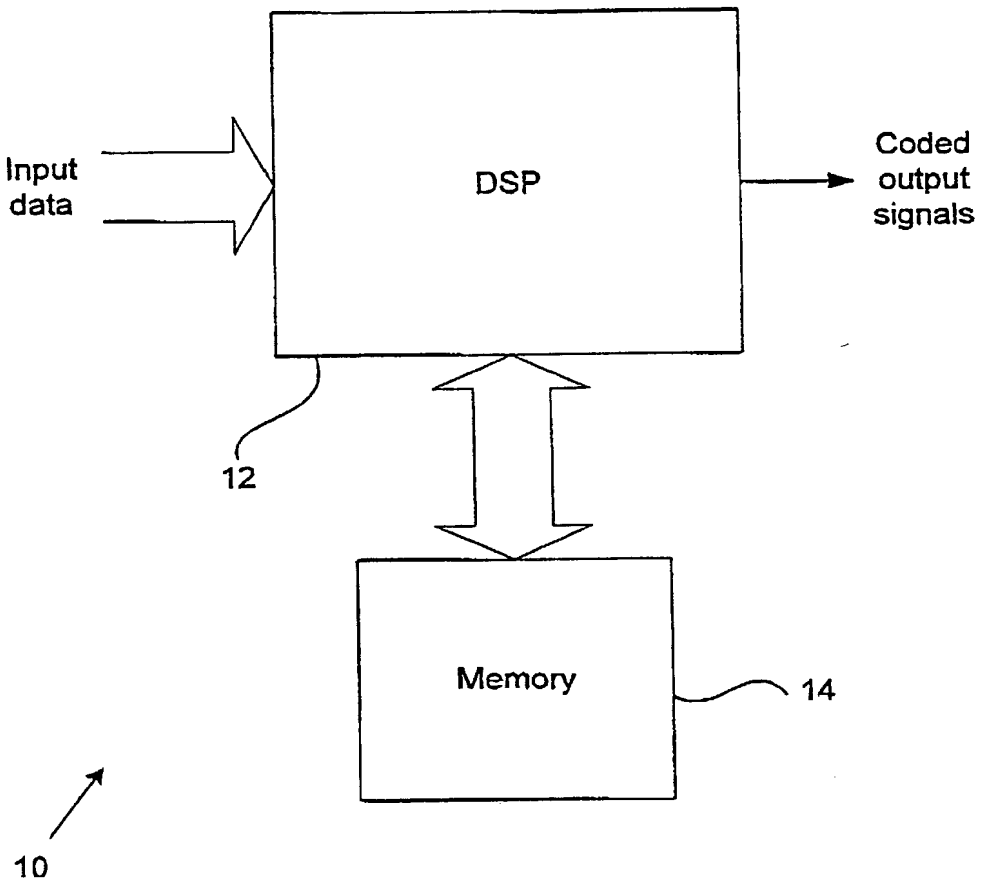

Figure 1

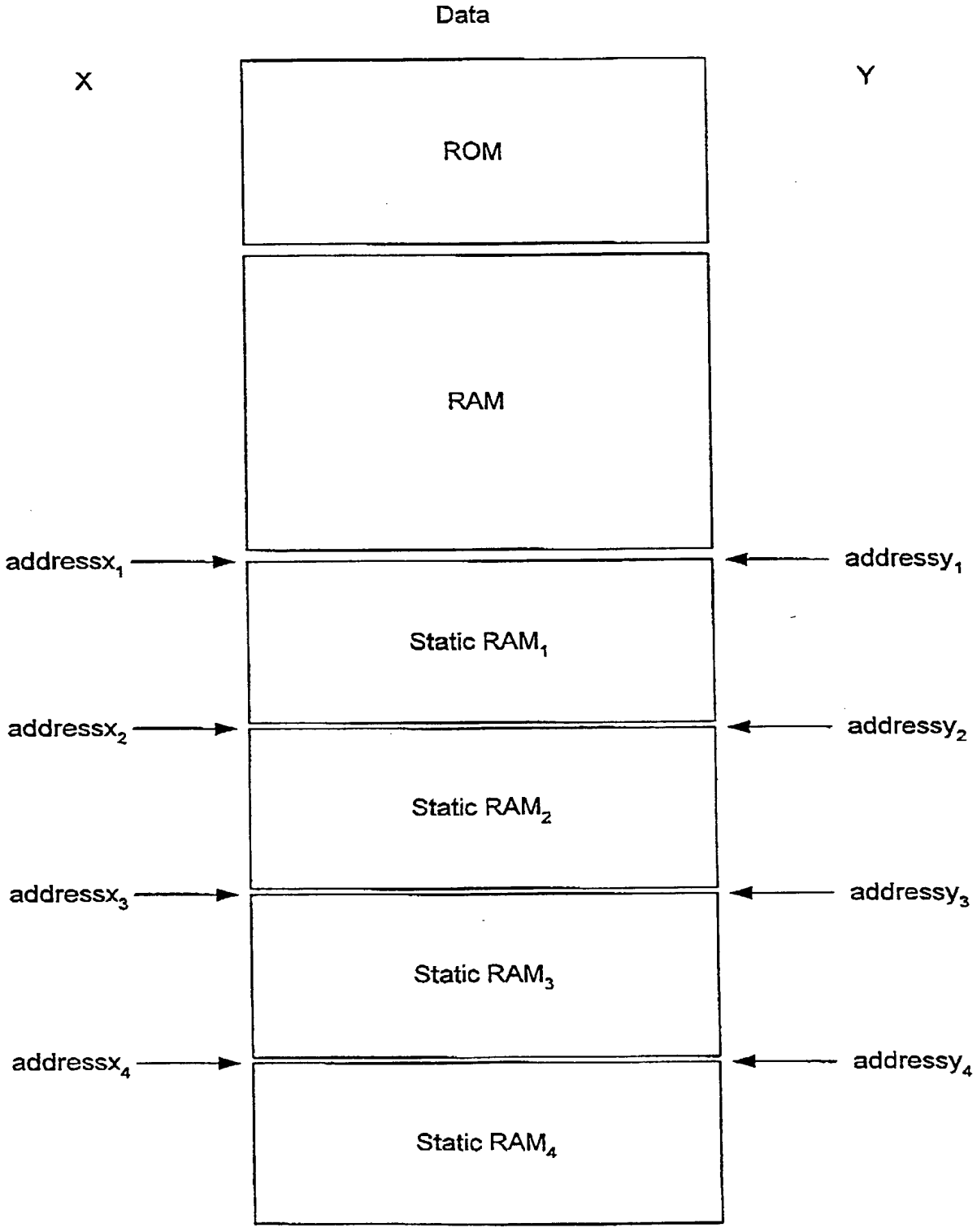

Figure 2

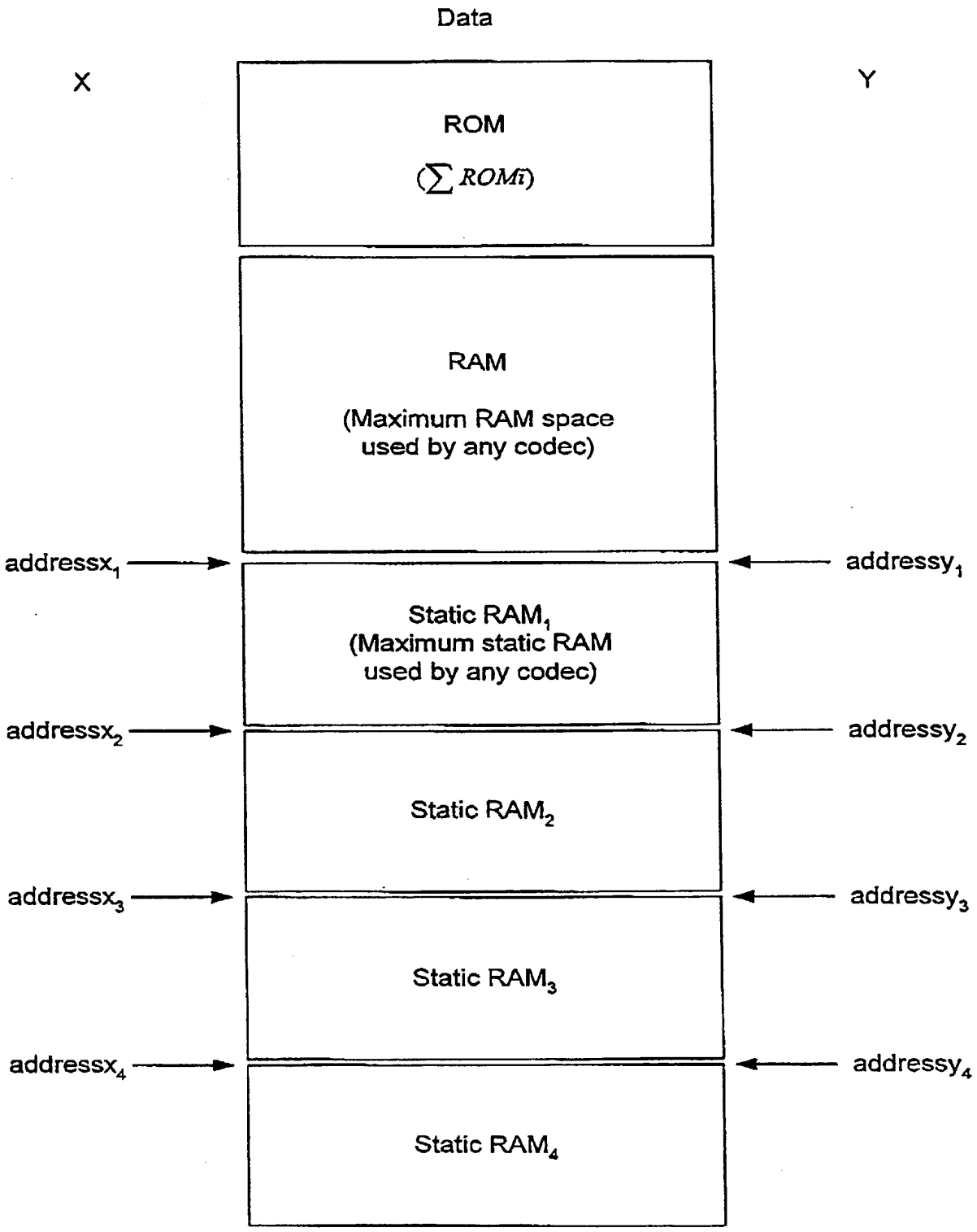

Figure 3

Please type a plus sign (+) inside this box [+]

PTO/SB/01 (10-01) (modified)

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
☐ Declaration Submitted with Initial Filing ☒ Declaration Submitted after Initial Filing	Attorney Docket No.	851663.434USPC
	First Named Inventor	Wenshun Tian
	COMPLETE IF KNOWN	
	Application Number	
	Filing Date	
	Group Art Unit	Not yet known
	Examiner's Name	Not yet known

As the below named inventor(s), I/we hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MULTIPLE INSTANCE IMPLEMENTATION OF SPEECH CODECS

(Title of Invention)

the specification of which was filed on (MM/DD/YYYY) **September 29, 1999** the specification of which is attached hereto ☐

as United States Application Number or PCT International Application Number **PCT/SG99/00095** Express Mail No.

and was amended on (MM/DD/YYYY) *(if applicable)*

I/we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

In addition, I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including material information which became available between the filing date of the prior application and the National or PCT International filing date of the continuation-in-part application, if applicable.

I/we hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Claimed	Certified Copy Attached? YES	NO
PCT/SG99/00095	WO	September 29, 1999	Y		X

Additional foreign application numbers are not listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I/we hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application No.	Filing Date (MM/DD/YYYY)	Application No.	Filing Date (MM/DD/YY)

Additional provisional application numbers are not listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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I/we hereby declare that all statements made herein of my/our own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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